sPHENIX Silicon Tracker Overview
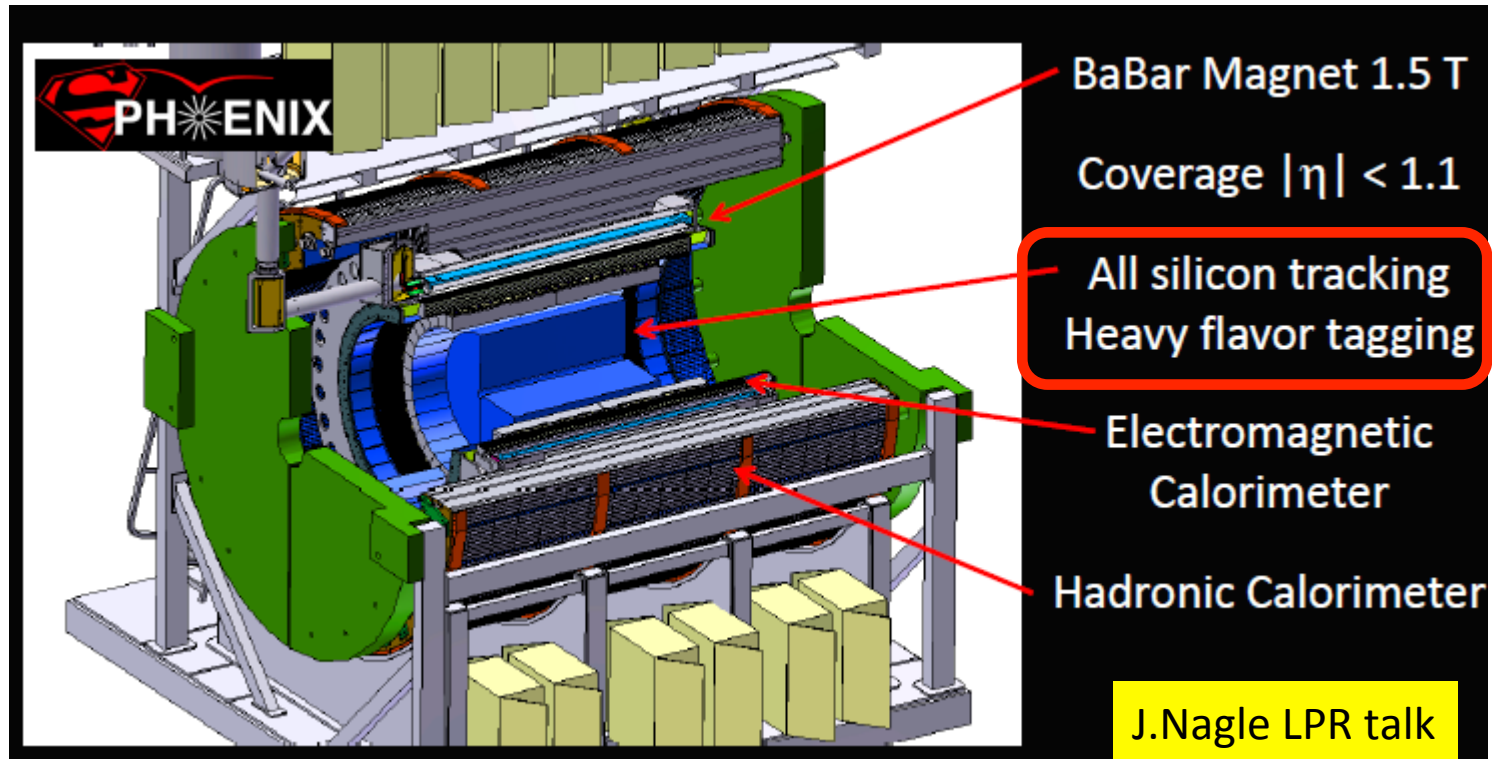
RIKEN/RBRC

Itaru Nakagawa

On behalf of sPHENIX Silicon Tracker Team

Reference design and requirements

BaBar Magnet 1.5 T

Coverage $|\eta| < 1.1$

All silicon tracking
Heavy flavor tagging

Electromagnetic
Calorimeter

Hadronic Calorimeter

J.Nagle LPR talk

- $|\eta|<1$ and $\Delta\phi=2\pi$
- High efficiency & purity in central Au+Au to measure modified FF
- High rate (15kHz DAQ)
- High momentum resolution to separate Upsilon states
- Precision vertex measurement for heavy flavor measurements (D, B$\rightarrow$J/Psi, b-tagged jets)
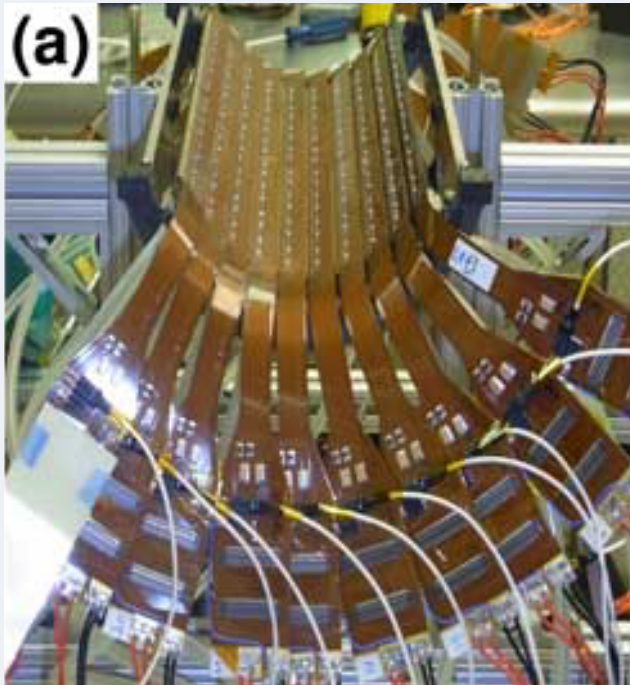- Compact (Fit inside of EMCAL)
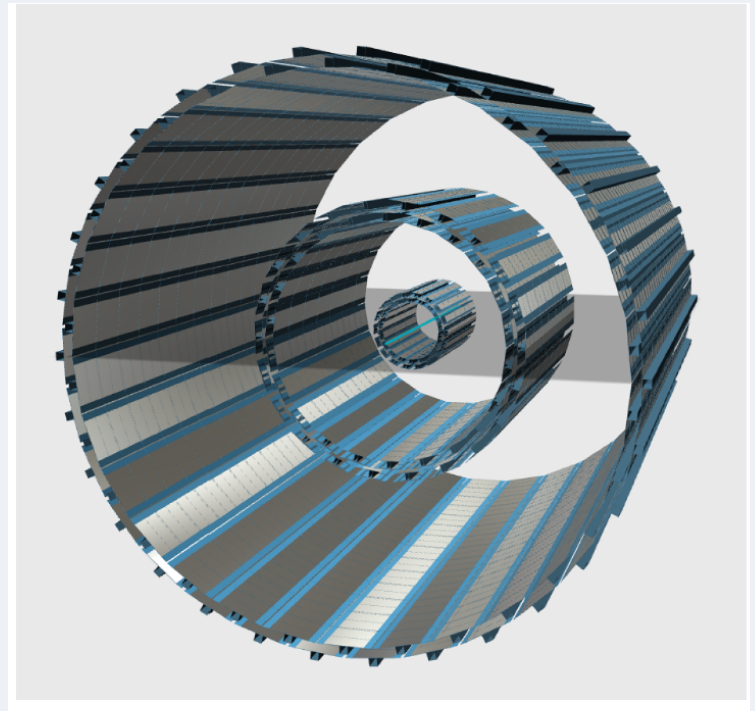
Inner + Outer Silicon Tracker

Inner Pixel	Outer Silicon Strip
2 Stations	3 Stations

PHENIX Pixel Sensors

Basic Project Philosophy

Basic Design Philosophy

Technology
- Employ existing technology
- Employ technology we are familiar with

Man Power
- Collaborate with Institutes which have the experience and infrastructure

Minimum Cost
- Little "R" and rather focus on "D"
- As compact as possible

Schedule
- **To be in time for 2020**

Current Model

Requirement

Specification

FPHX

Outer Radius ~ 60cm

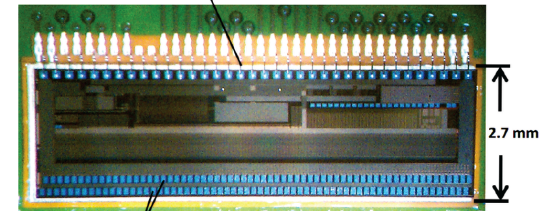No Stereo Angle

Single Sided Strip Sensor

AC Coupled

<100MeV Resolution for Upsilon

FVTX Silicon Module for PHENIX

1 cm

A072

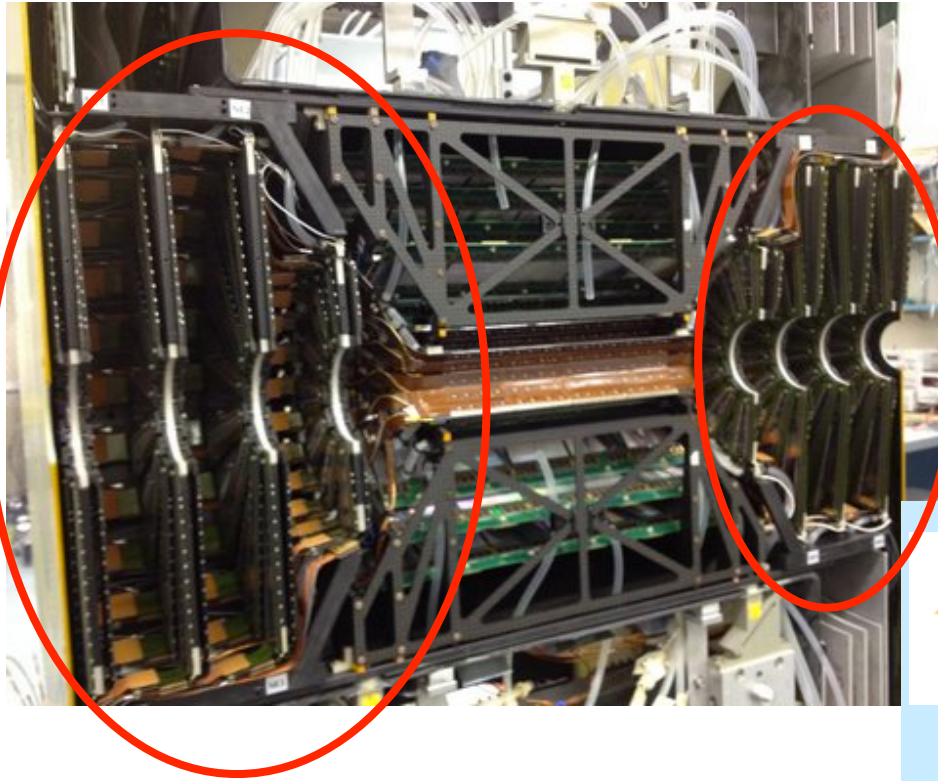Wire bonds to HDI for chip I/O, power, and ground
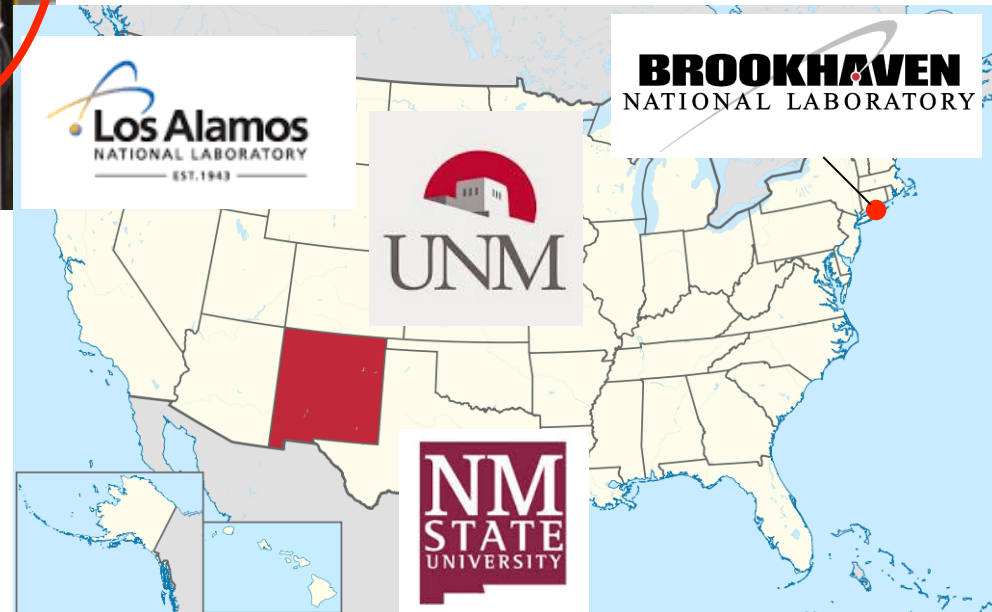
2.7 mm

Bond pads to strips

FPHX Chip

Existing technology which satisfies the requirement

Existing FVTX Detector

FVTX Project	2006 - 2008	2008 - 2011
R &D	→	
Construction		→

Technology and Resources are still in New Mexico & BNL

Existing PIXEL Detector
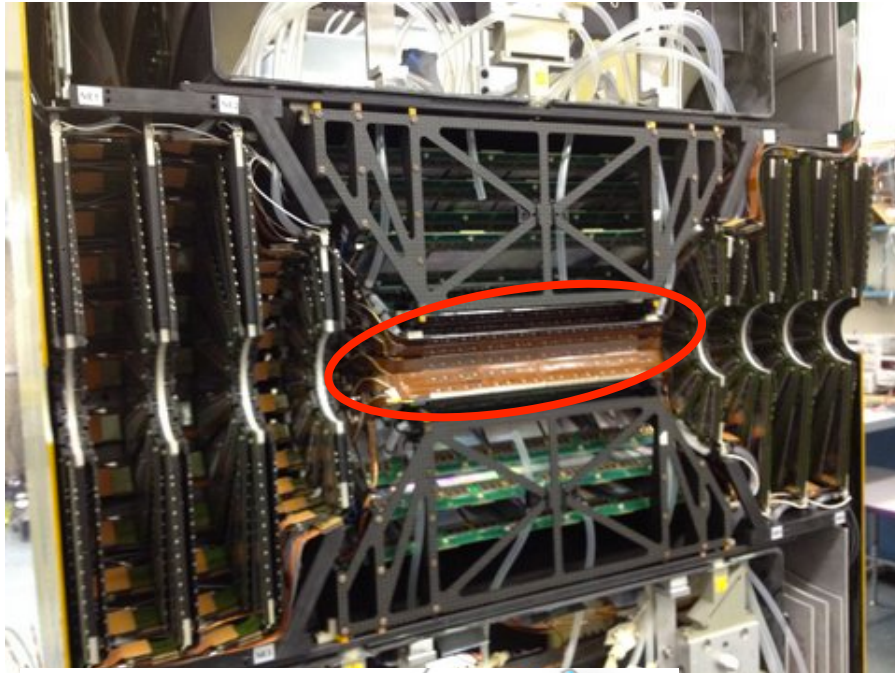
FVTX Project	2003 - 2007	2007 - 2010
R &D	→	
Construction		→

Technology and Resources are in RIKEN & BNL

Silicon Tracker Developing System
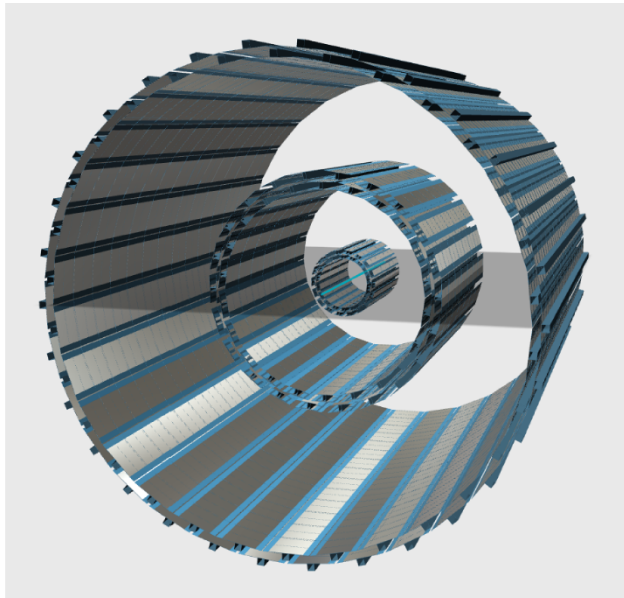
FVTX Project	2014 - 2018	2018 - 2020
R &D		
Construction		

Eastern Asia + NM + BNL Collaboration
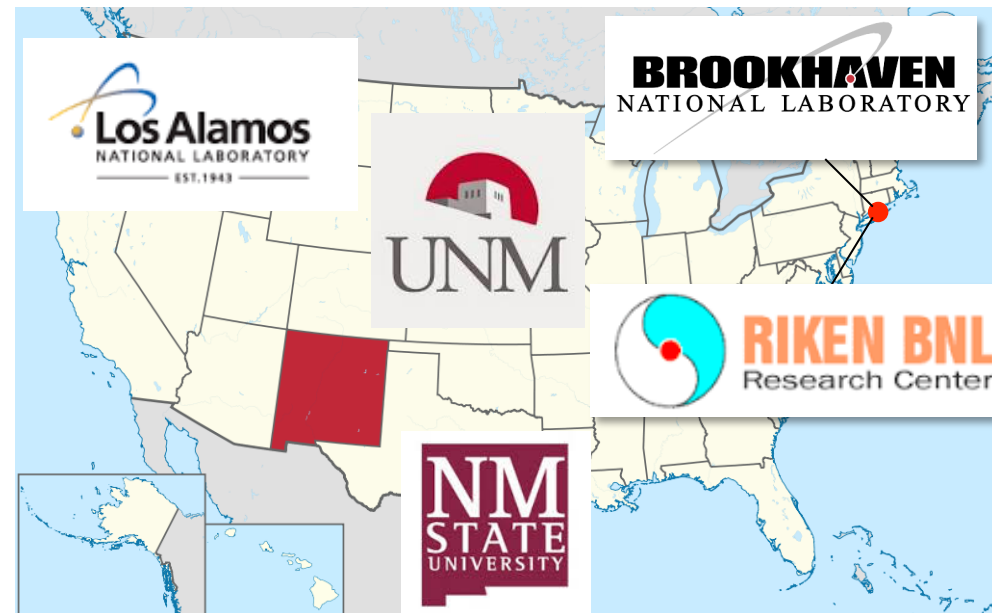
FPHX Chip

Specification	FPHX	SVX4
ADC/channel	3 bits	8 bits
Power Consumption	64 mW	300 mW
Cooling	Air	Liquid

Material	Less	More
Cooling Operation	Less risky	More risky

Readout Electronics

FVTX Readouts

Wedge · BCO · ROC · FEMIB · FEM
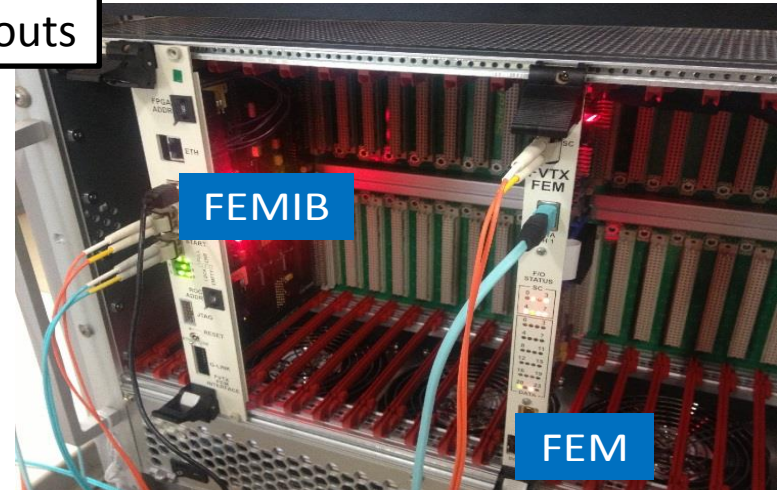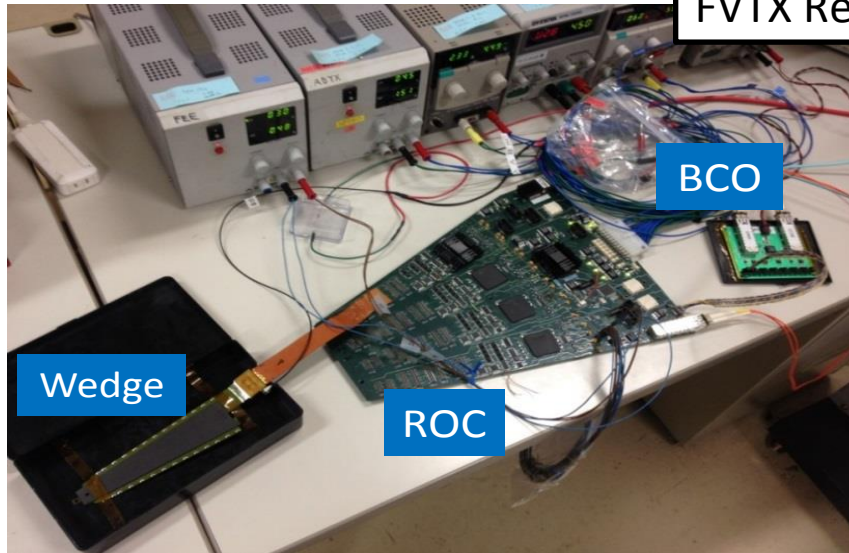
HDI for FVTX

HDI for sPHENIX Si Tracker
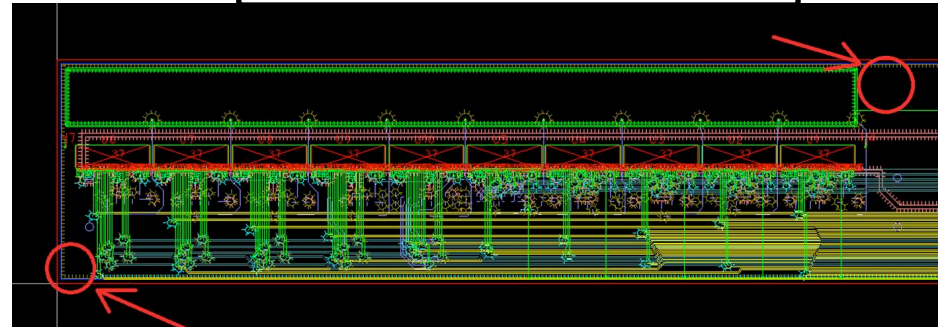
- Electrically same design with FVTX's and even less technologically challenging.
- Rest of readout electronics will be very similar to these of FVTX

Silicon Tracker Model

- 5 strip layers + 2 pixel

    S2:   1 strip layer at R~64 cm ~1% X0   (2% in ref. design)

    S1ab: 2 strip layer at R~32 cm 1.2% X0 total (2% in ref. design)

    S0ab: 2 strip layer at R~ 8 cm ~2% X0 total (2.7% in ref. design)

    P1:   pixel at R~5 cm   (reconfigured VTXP) 1.3% X0

    P0:   pixel at R~2.5cm (reconfigured VTXP) 1.3% X0

    – All strips are 60 or 58 μm x 9.6mm. No stereo

    – Overall material is ~4.2% (+ 2.6% pixel) radiation length.
        Most of them (~3%+2.6%) are near beam or in the last layer

    – Small rad. length to make small over-all size and to keep the required momentum resolution to separate 3 Upsilon states

    – S0+S1+S2: ~10m^2 of silicon and 3.1 M ch

Current design in pCDR

Station	Layer	radius (cm)	pitch (μm)	sensor length (cm)	depth (μm)	total thickness $X_0\%$	area (m^2)
Pixel	1	2.4	50	0.425	200	1.3	0.034
Pixel	2	4.4	50	0.425	200	1.3	0.059
S0a	3	7.5	58	9.6	240	1.0	0.18
S0b	4	8.5	58	9.6	240	1.0	0.18
S1a	5	31.0	58	9.6	240	0.6	1.4
S1b	6	34.0	58	9.6	240	0.6	1.4
S2	7	64.0	60	9.6	320	1.0	6.5

Table 4.2: Number of channel summary for the silicon strip tracker.

station	sub-layer	silicon modules per ladder	# of ladders	# of sensors
S0	2	3	36	216
S1	2	7	44	616
S2	1	14	48	672

Simulation of the current design (in pCDR)

Y(1S,2S,3S) → e⁺e⁻

$$\frac{\Delta p_T}{p_T} = \sqrt{(1.18\%)^2 + (0.061\%)^2 p_T^2}$$
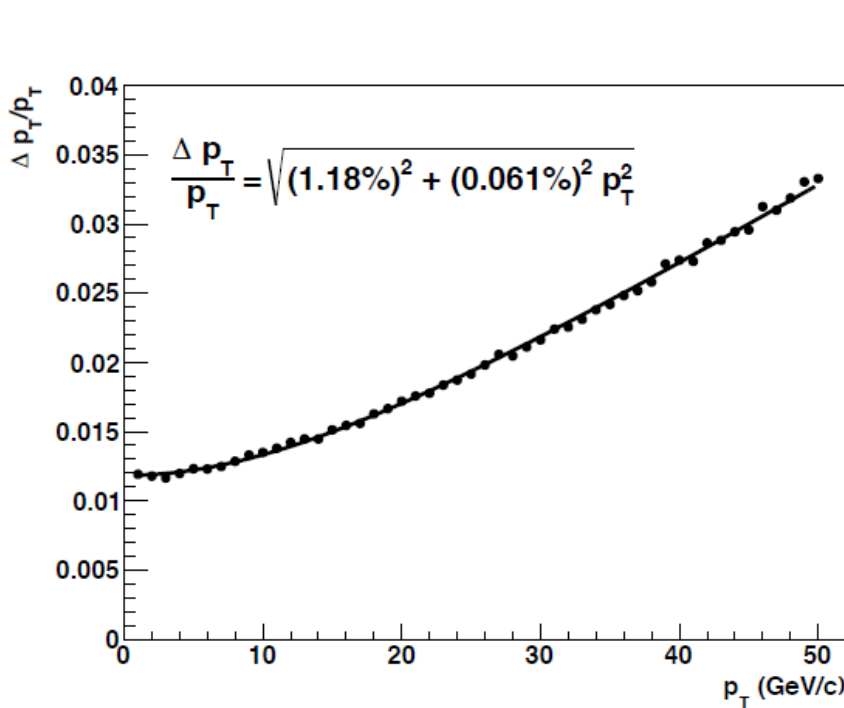
Figure 4.41: Momentum resolution of the silicon tracker for single pi(
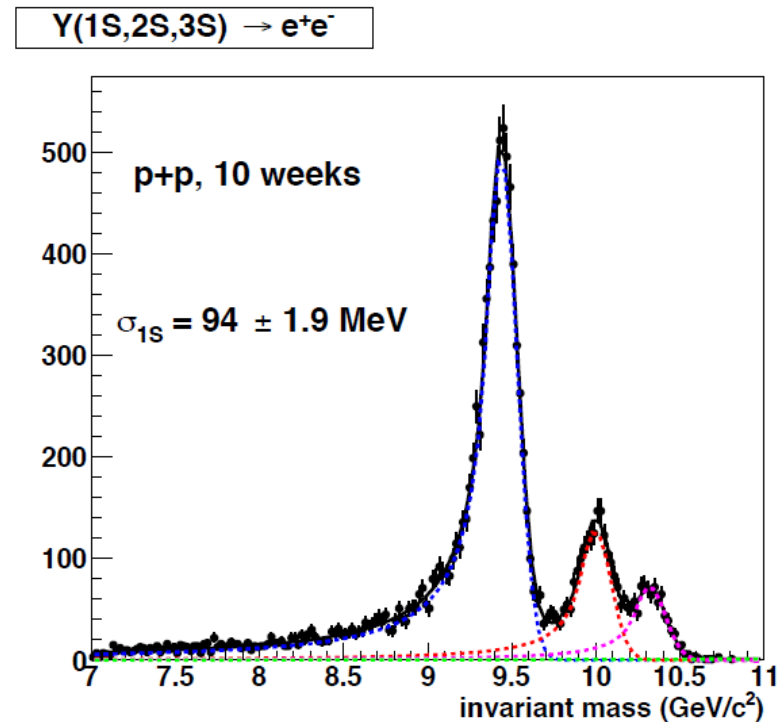
p+p, 10 weeks

$\sigma_{1S} = 94 \pm 1.9$ MeV

Figure 4.42: Mass spectrum of the three Upsilon states, with Crystal Ball fits.

- Expected momentum resolution and mass resolutions for Upsilon calculated by Tony Frawley for preliminary Conceptual Design Report

- $\sigma=94$ MeV for Upsilon. Three upsilon states are clearly separated
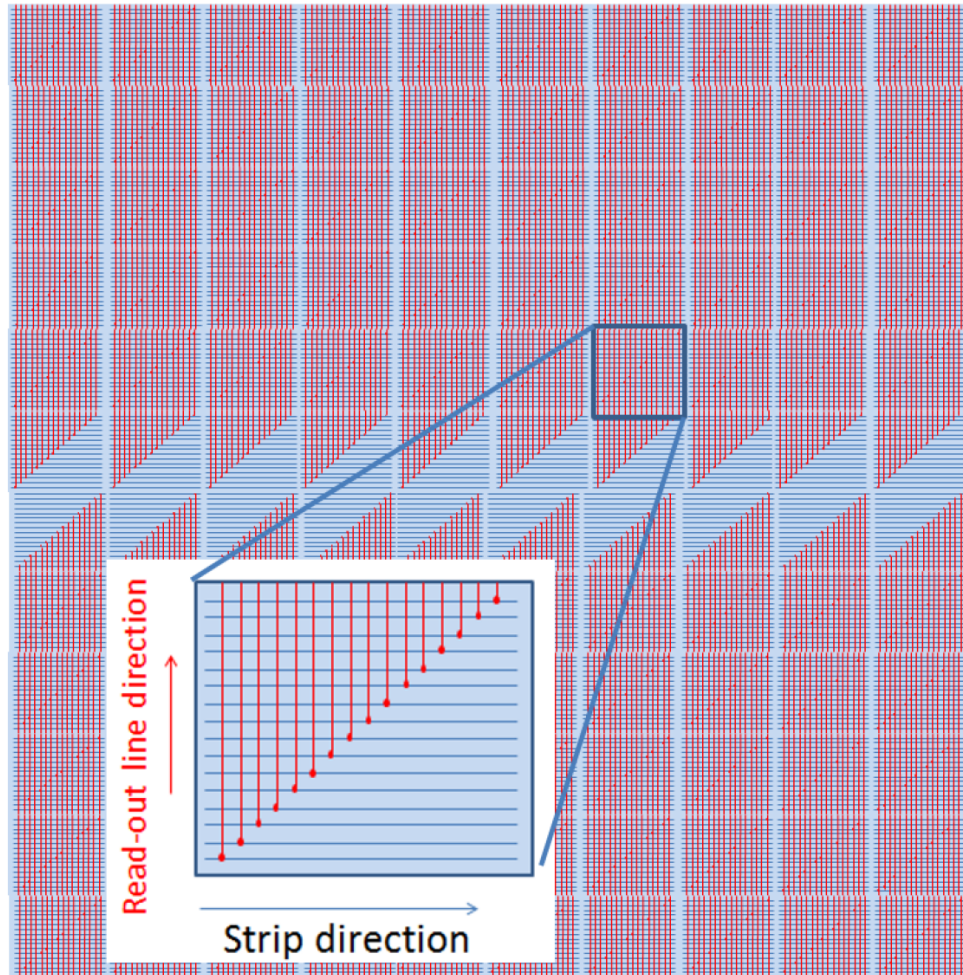
Concept of Sensor (for S2)

Figure 4.3: Schematic layout strip and readout lines of the sensor.

- 96mmx92.16mm active area
- Divided into 10x12 blocks
- Each block is 9.60mm x 7.68mm and made of 128 strips of 9.6mm x 60 micron
- Upper 6 bocks are connected upwards.
- Lower 6 blocks are connected by downwards
- 24 FPHX chips to read-out the entire sensor

3 sensors for strip layers
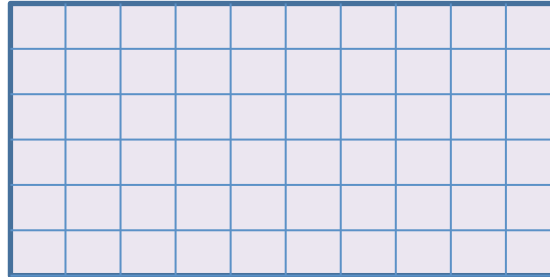
S2 sensor

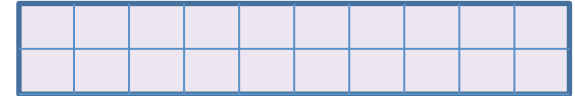Bonding pads for 10 FPHXs
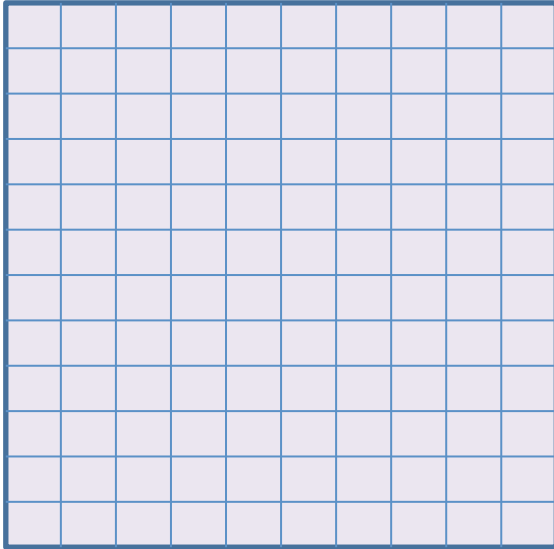
Bonding pads for 10 FPHXs

S1 sensor

Bonding pads for 10 FPHXs

Bonding pads for 10 FPHXs

Bonding pads for 10 FPHXs

Bonding pads for 10 FPHXs

- Each sensor is divided in cells of 9.6m(z)x7.68mm active area. Each cell consists of 128 strips of 60μm x 9.6mm
- S2, S1, S0 sensors are made of 12x10, 6x10, and 2x10 cells, respectively
- 1 ch in S2 read 6 strips and 1 ch in S1 read 3 strips to save channel counts. Channel occupancy is ~0.2% in S1 and 0.1% in S1 in central Au+Au.

Concept of FPHX based module (S1)

HDI of 10 FPHX chip
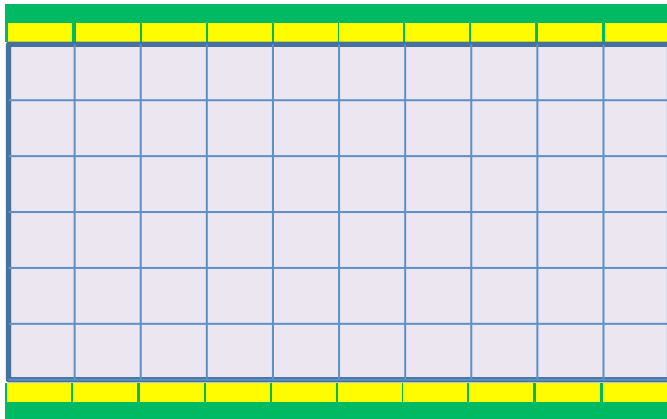
HDI of 10 FPHX chip

- This is a concept of a sensor module with FPHX read-out
- It is made of
  - Sensor of (6 x 10) cell structure. Each cell has 128ch of 58 um x 9.6mm strips
  - A "ROC" (or "HDI") of 10 FPHX chips. They are attached at the top and the bottom of the sensor
  - The "HDI" is electrically equivalent to the "small HDI" of FVTX so that it can be read-out by a FVTX test bench
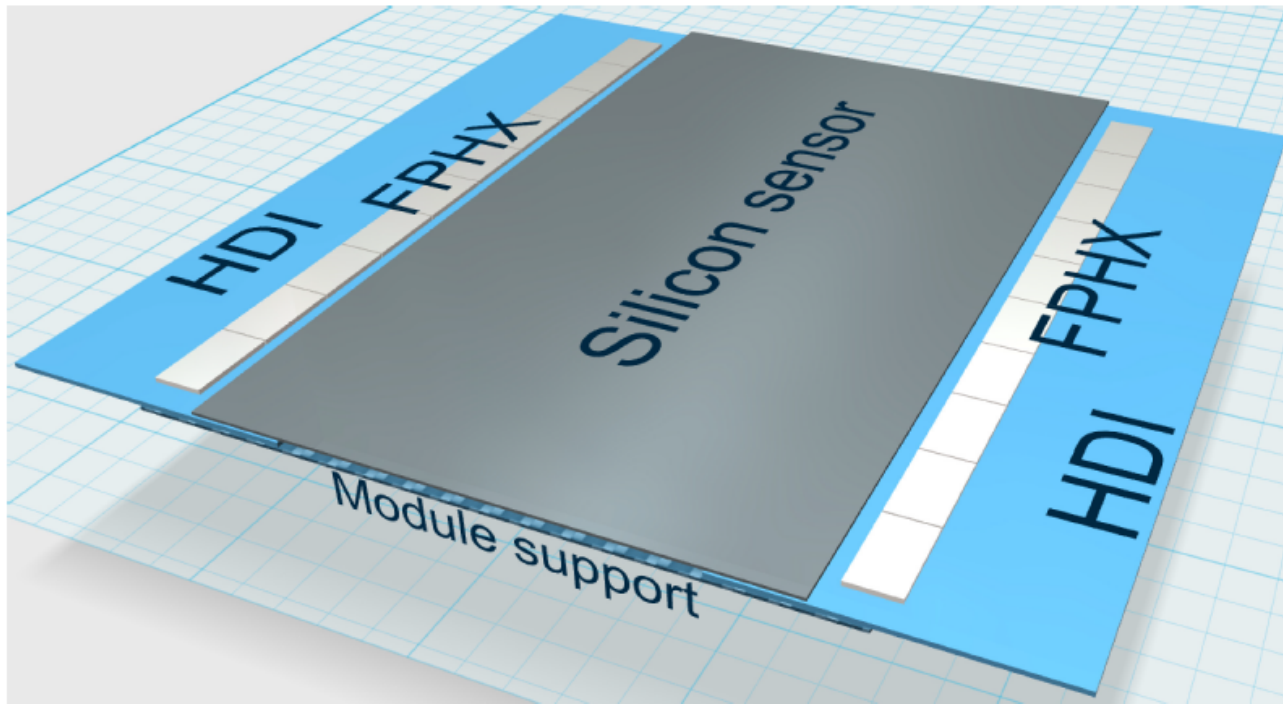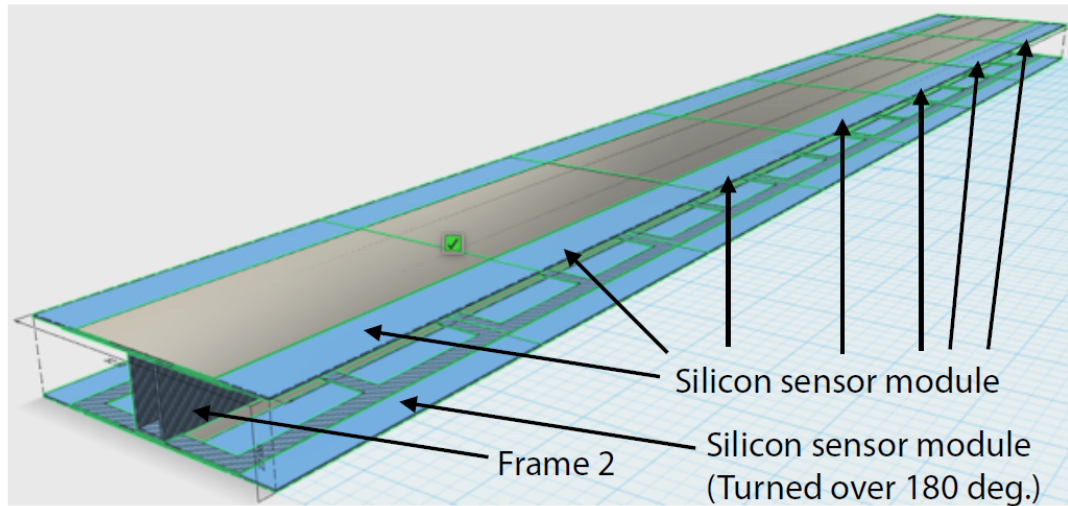
S1 Silicon Module

Figure 4.48: Layout for the silicon sensor module for the S1 detector.

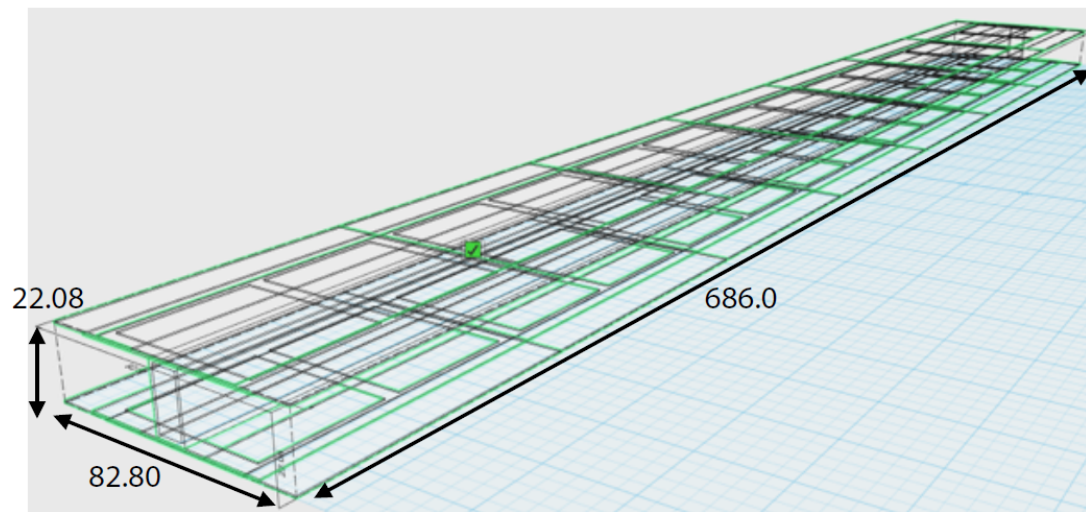# S1 ladder

side view (outline&material)

Cooling tube position will be optimized

Silicon sensor module

Frame 2

Silicon sensor module (Turned over 180 deg.)

side view (outline)

22.08

686.0

82.80

S0 barrel (R~8cm)

$\varphi_{offset}=2\pi/36$ $\varphi=2\pi/18$

102.24
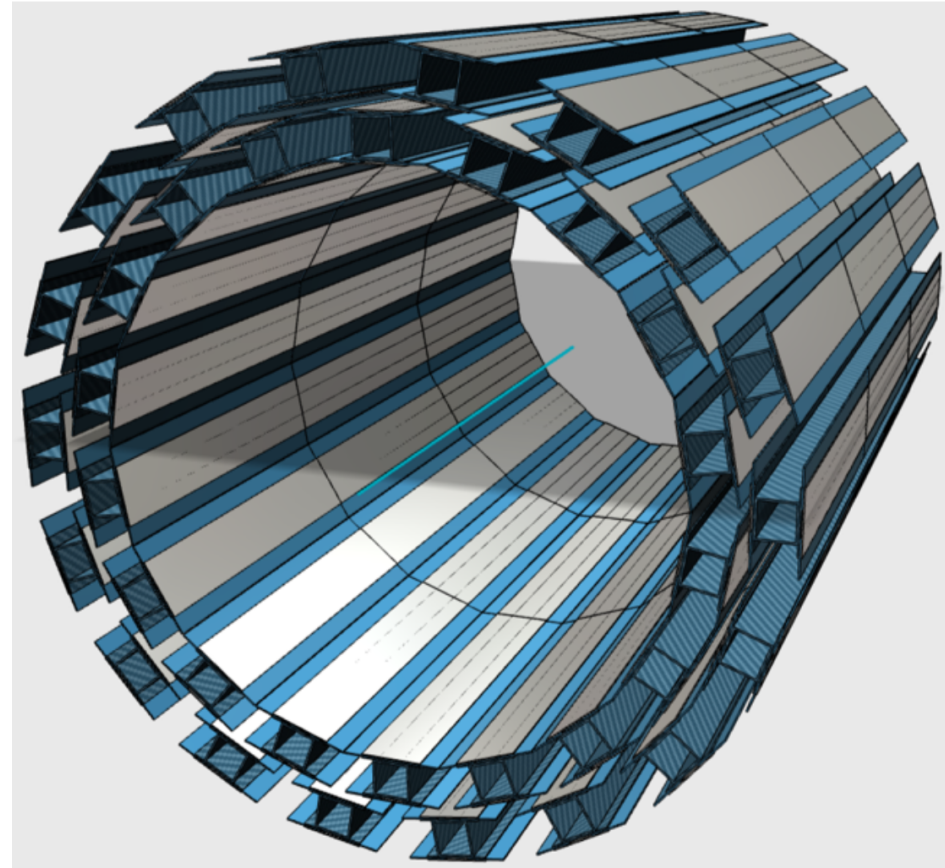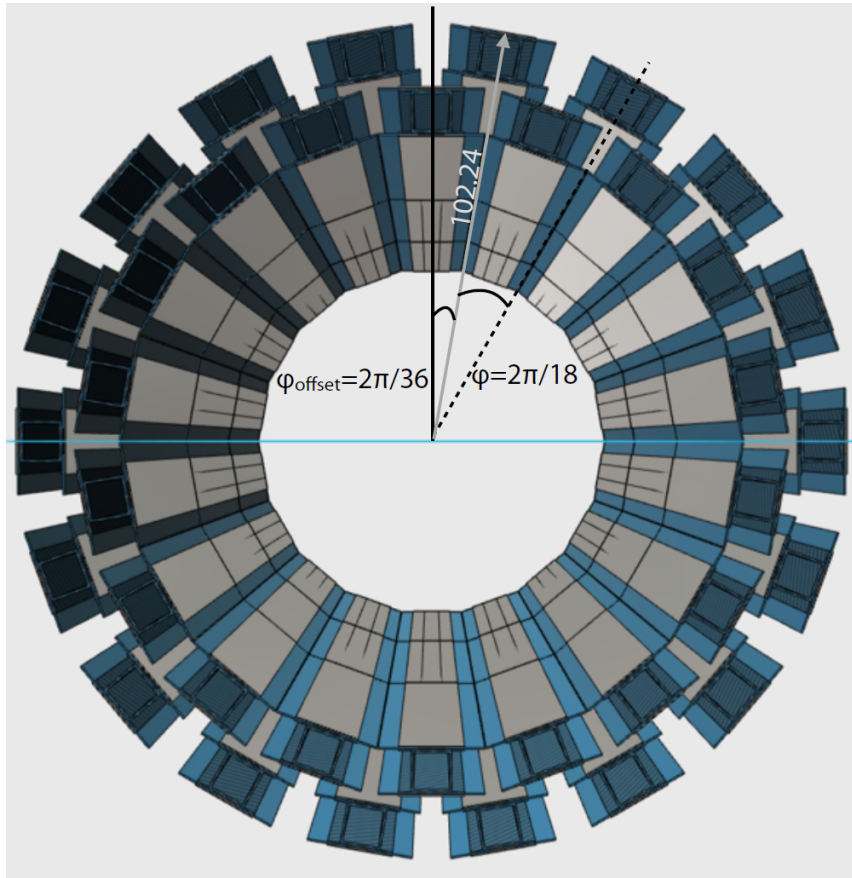
- Two Layers Staggered to Cover the Dead Area
- Tight spatial constraint. Rather challenge in HDI design.

S1 barrel (R=30-35cm)

- Two Layers Staggered to Cover the Dead Area
- Less spatial constraint. Conservative HDI design.

S2 (R~65 cm)

- Single layer.
- Least geometrical constraint.

S0, S1, S2 Barrels

- Design of the support structure has not started yet.

Time line of the project

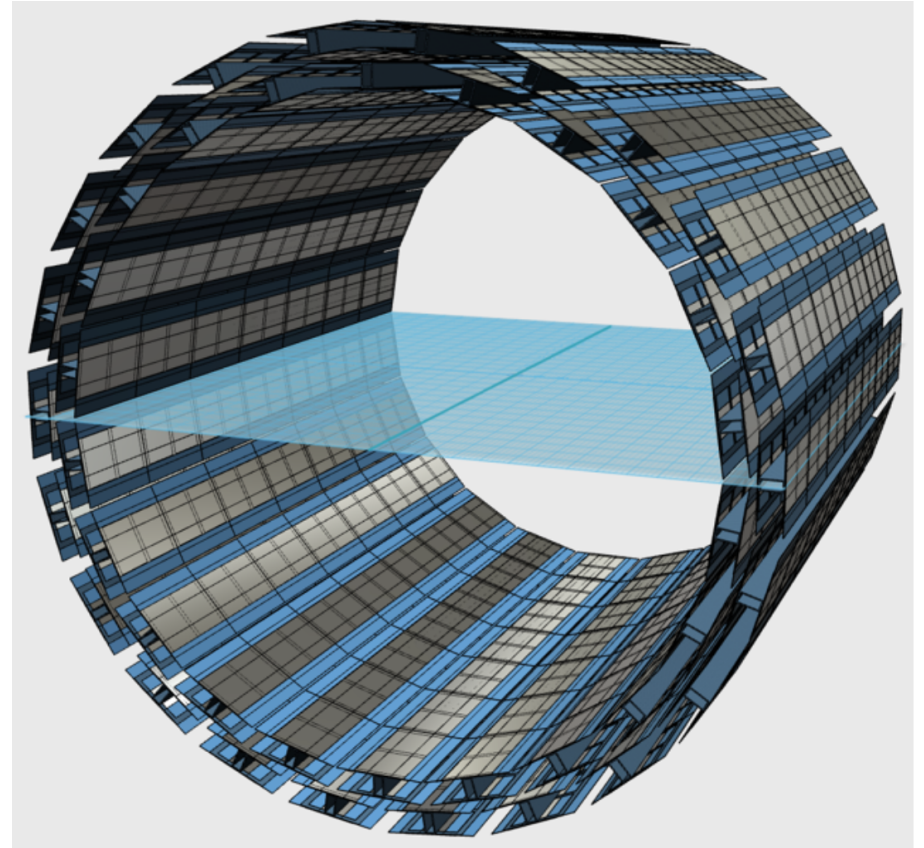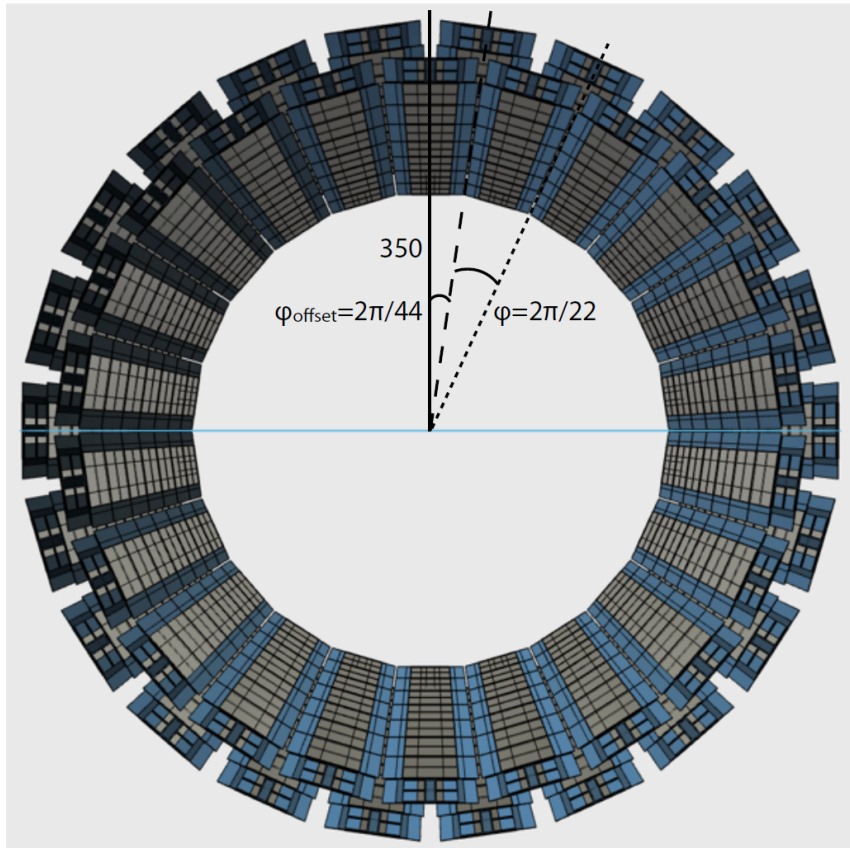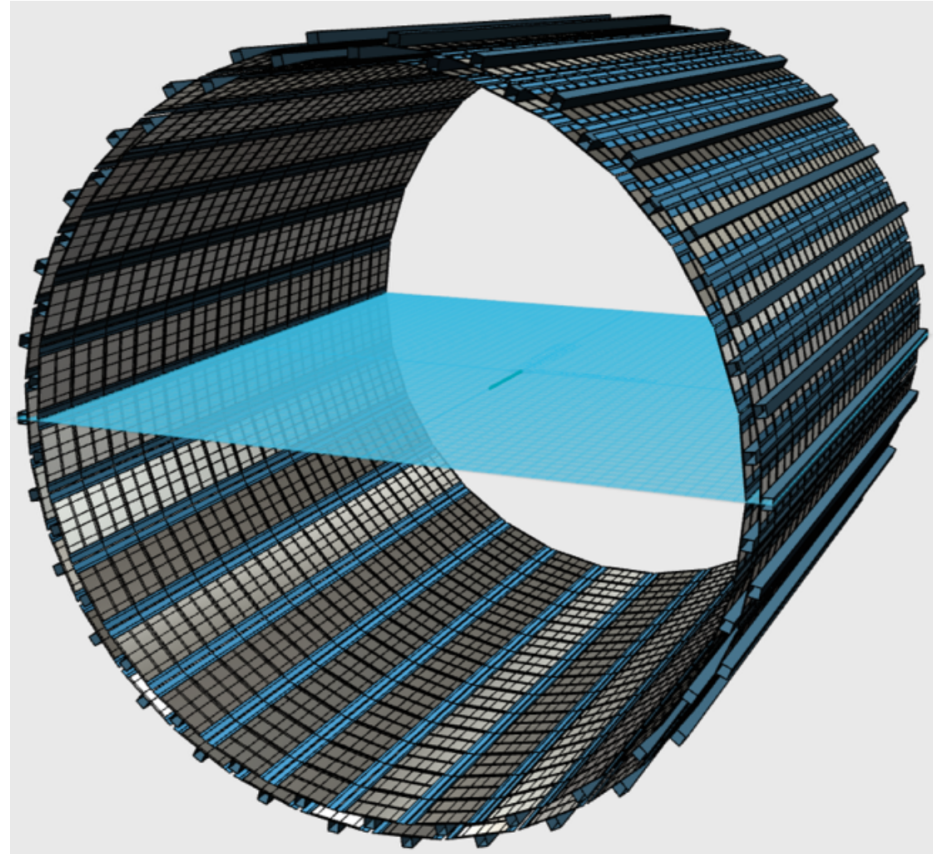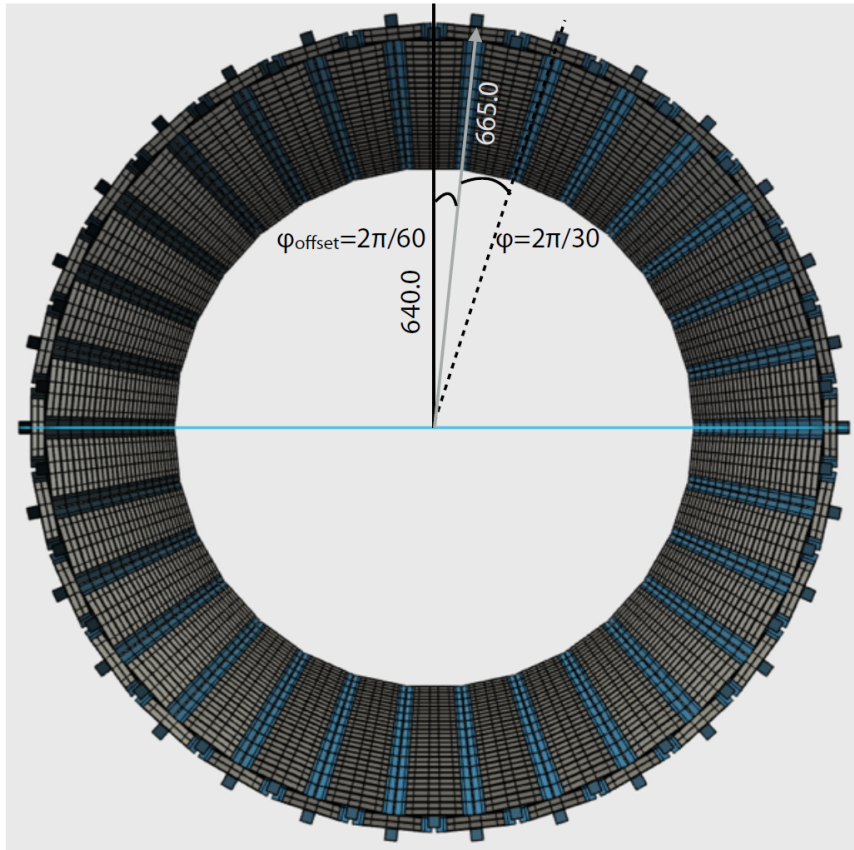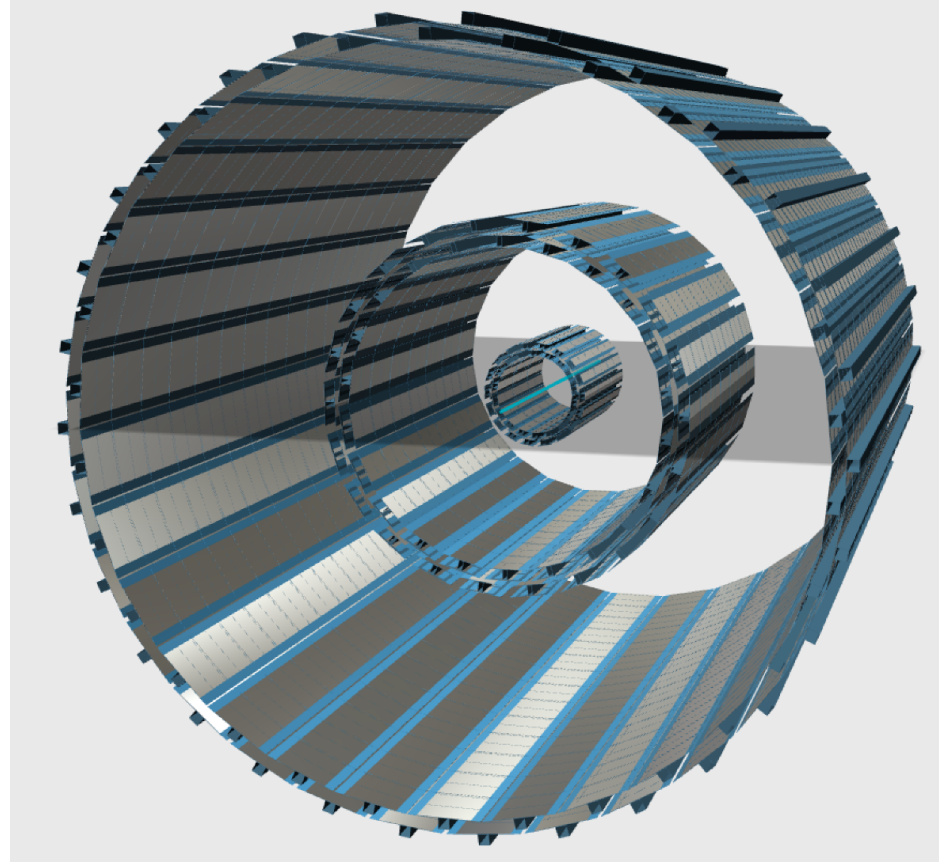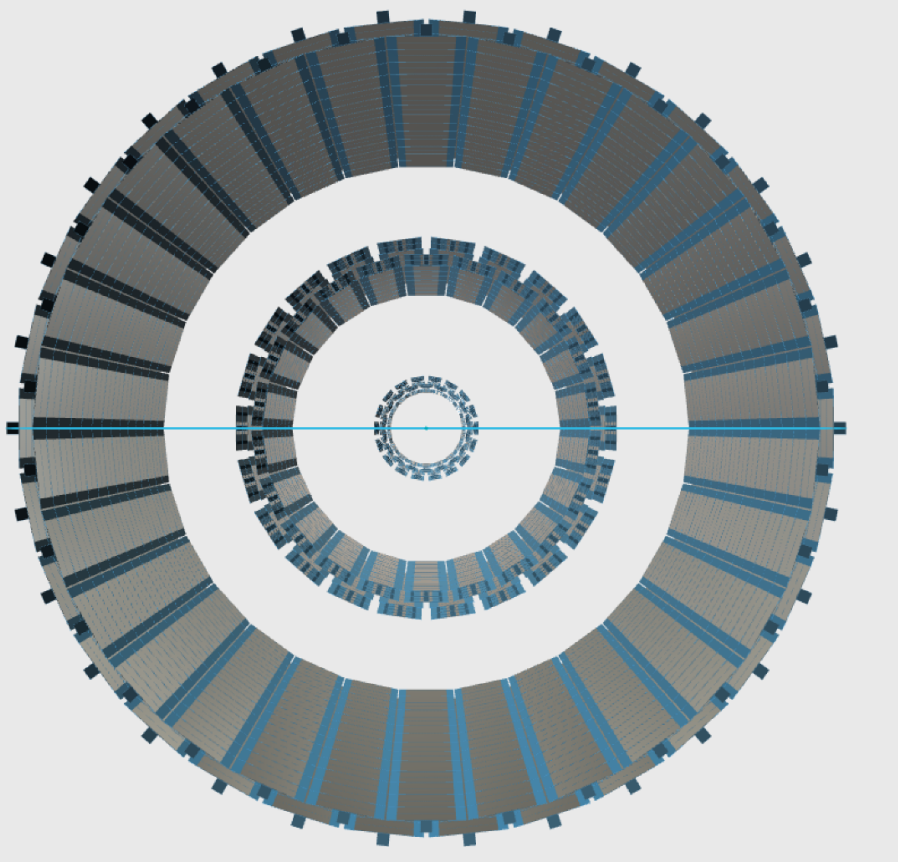|	2015		2016				2017				2018				2019				2020				2021			
	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Mechanical System Design	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓													
Si Module													▓	▓	▓	▓	▓	▓	▓						
Preproduction								▓	▓	▓	▓	▓													
Ladder									▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓						
Layer													▓	▓	▓	▓	▓	▓	▓			▓	▓		
Electronics																									
Asic					▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓						
ROC					▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓						
FEM					▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓	▓								

Prototype (light green)   Production (dark green)

Si Strip Detector Labor Profile

All Labor

SPHENIX SISTRIP BUDGET PROFILE

Direct FY16$

Legend: Labor | M&S

- 2016: $354,000
- 2017: $111,500
- 2018: $3,317,500
- 2019: $934,000
- 2020: $12,000
- 2021: $9,000
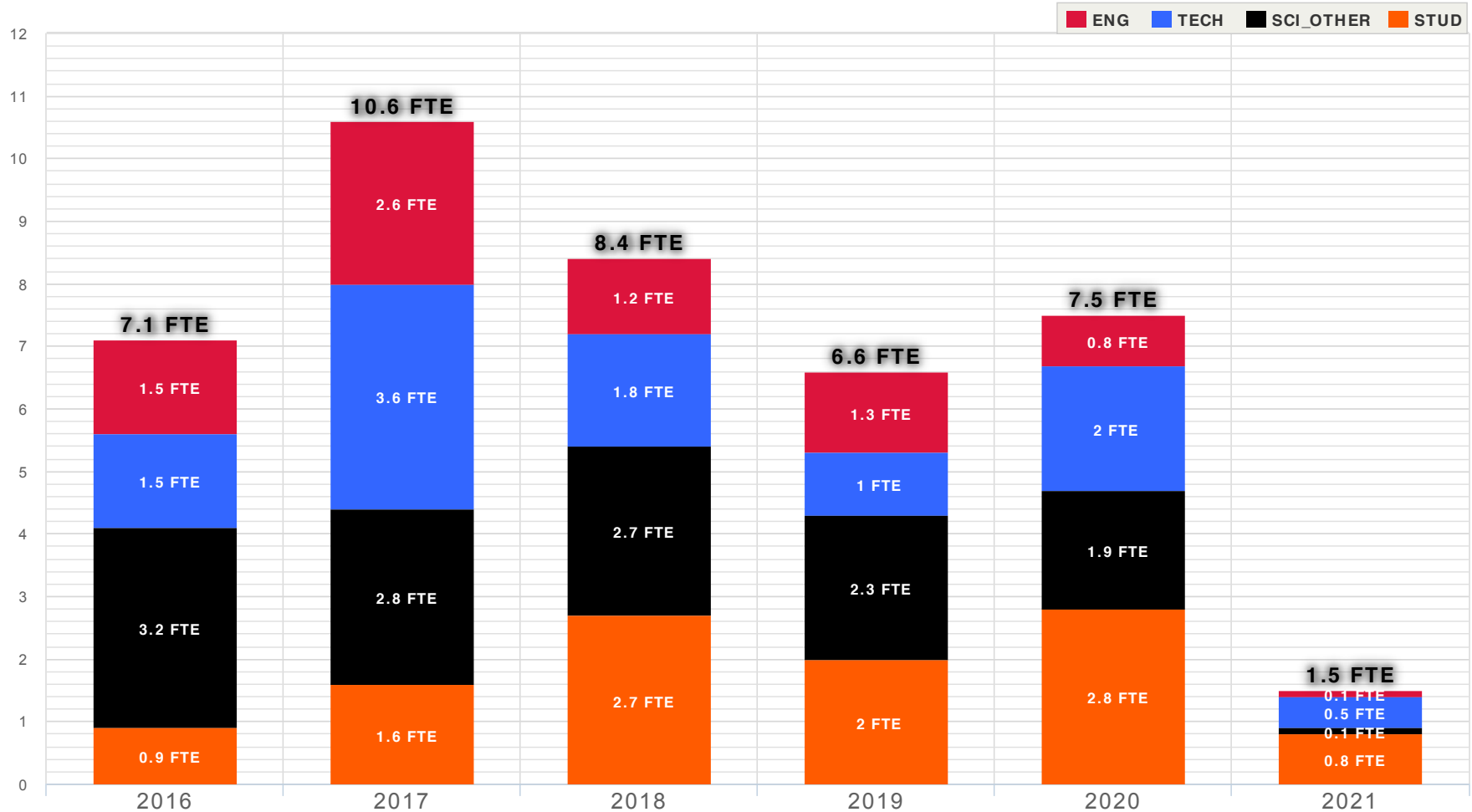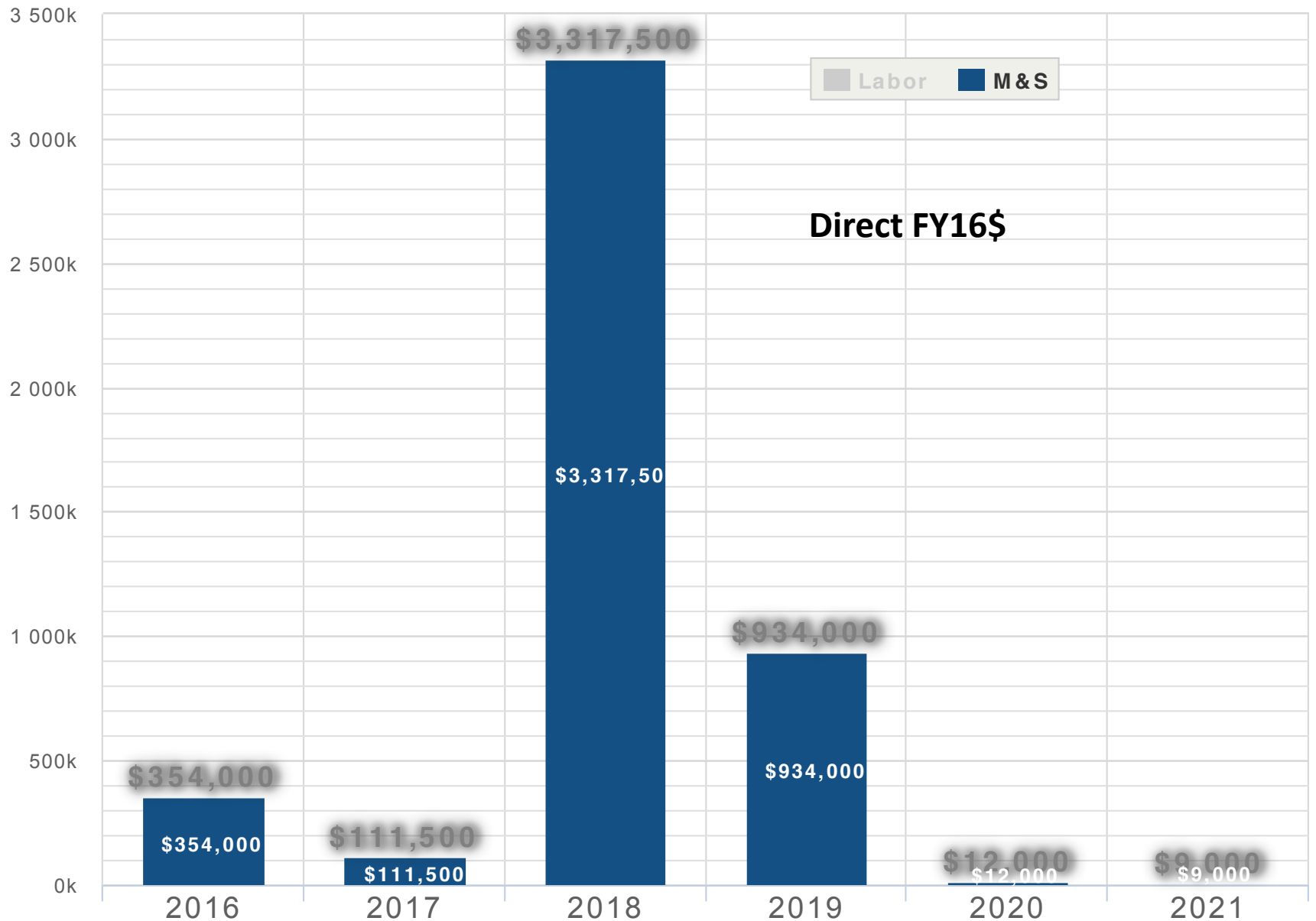
Highcharts.com

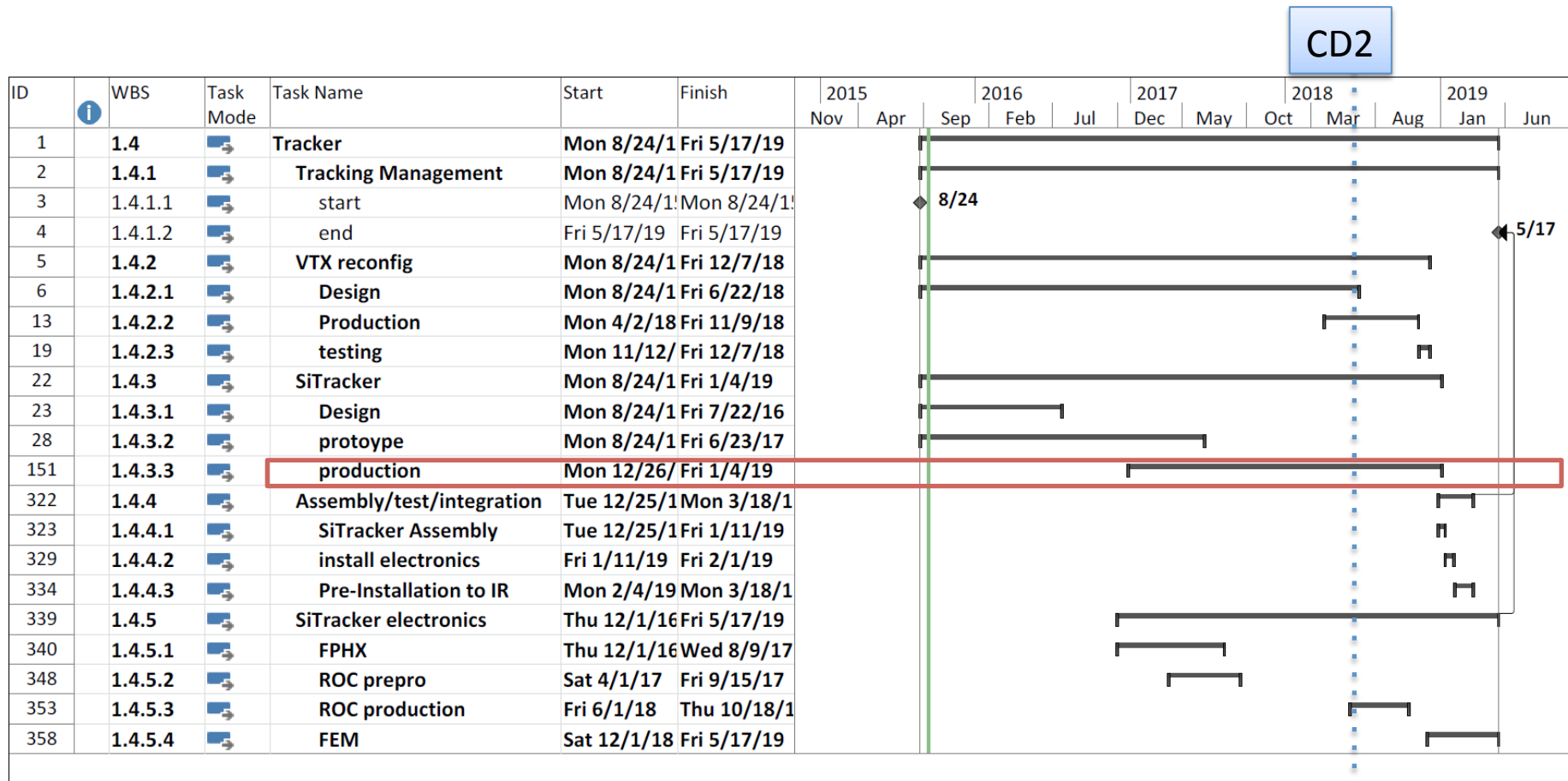# Aggressive Time line of the project

According to the current status of prototyping, the production can be started earlier. This will smear concentrated budget of Y2018 to earlier years.
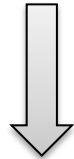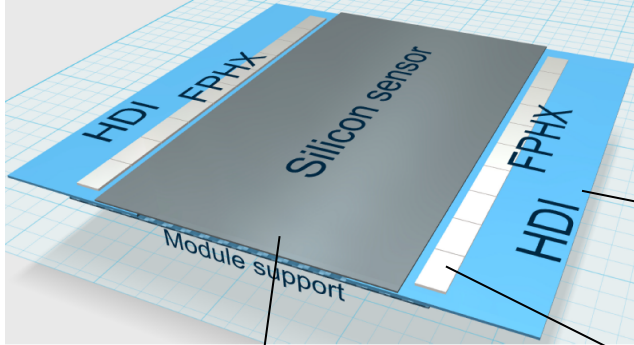
Requested funding profile to JSPS

Unit: 100K yen ~ $1K	JFY2016	JFY2017	JFY2018	JFY2019	JFY2020	Total
Prototype	300	0	0	0	0	300
FPHX	200	0	0	0	0	200
Sensor production	0	660	660	401	0	1721
Ladder assembly	0	335	366	245	128	1074
ROC/FEM	0	0	0	300	450	750
Misc	20	40	40	40	40	180
Total	520	1035	1066	986	618	4225

- The budget profile of the M&S of Si-Tracker in the grant proposal
- The Grant cover prototype and M&S of the tracker hardware
  - JFY2016   Prototyping of ladders (S0,S1,S2)
  - JFY2017-2019   production of sensor and ladders
  - JFY2019,20 ROC/FEM
- Complete the tracker by the first half of JFY2020 (Sep 2020)
- NOTE: RIKEN/RBRC personnel will work on the project, but not in the JSPS funding request above.

Production Scenario

HDI FPHX

Silicon sensor

FPHX

HDI

Module support

Fermilab

YAMASHITA MATERIALS

スピードと信頼を技術で支えるサーキテックカンパニー

設計・プリント基板・実装・組み立ての電子機器一貫生産体制に
「スピードと信頼」を加え、地球環境の保全に配慮しながら
お客様のあらゆるニーズにお応えしています。

HAMAMATSU
PHOTON IS OUR BUSINESS

HAYASHI

Assembly

Suburb of Tokyo
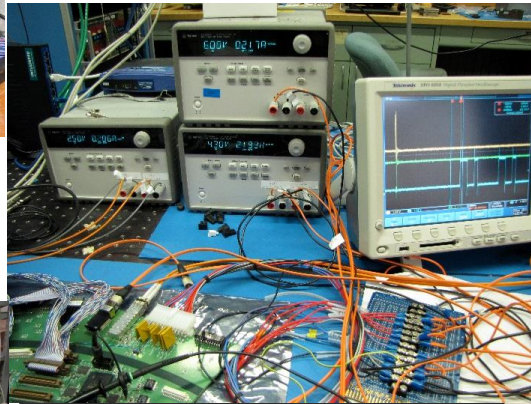Performed PIXEL Assembly

Testing Facility
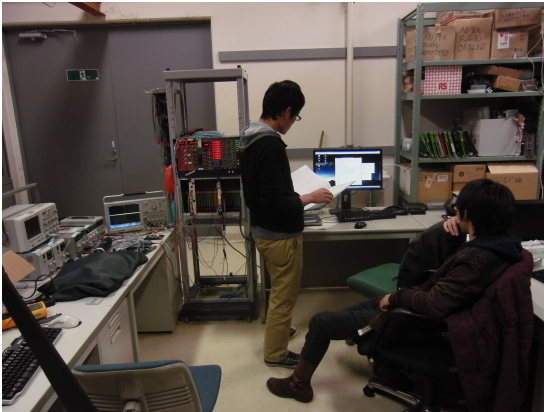## Manpower Expertise and Availability

UNM

FVTX benches' test can be used immediately to test Si Strip modules (use FPHX). They can be used to test prototype Si strip module/ladder.

LANL

RIKEN

BNL